What is claimed is:

1. A fault tolerant computer comprising: a processor to execute instructions, said processor including instructions to execute an original and mirror instructions to produce results to be compared in a redundancy routine, a radiation hardened comparison circuit coupled to compare an original result and a first mirror result, said comparison circuit providing an output of a first state when said original result agrees with said mirror result and an output of a second state when said original result and said mirror result disagree, said second state comprising an SEU error signal.

2. A fault tolerant computer according to claim 1 wherein absence of an original or mirror result comprises disagreement with the other result.

3. A fault tolerant computer according to claim 1 wherein said comparison circuit output is coupled to inhibit production of additional mirror results when said output is in the first state.

4. A fault tolerant computer according to claim 3 wherein said processor is provided with instructions to perform an SEU recovery routine in response to detection of an SEU error signal.

5. A fault tolerant computer according to claim 4 wherein said processor comprises means for storing the original result and the mirror result in response to an SEU error signal, means coupling the SEU error signal to command production of a next original result and a next mirror result, coupling means coupling said original result for comparison with said next original result by said comparison circuit and coupling said mirror result for comparison with said next mirror result by said comparison circuit and said comparison circuit comprising means for producing a signal of the first state when at least one of the original result and next original result or the mirror result and next mirror result match to allow use of a result matching a next result by said processor.

6. A fault tolerant computer according to claim 5 wherein allowing use comprises transmitting the result to a processor bus.

7. A fault tolerant computer method comprising: executing an original and mirror instructions to produce an original and a mirror result respectively to be compared in a redundancy routine, comparing said original and mirror results in a radiation hardened comparison circuit, and providing an output of a first state when said original result agrees with said mirror result and an output of a second state when said original result and said mirror result disagree, said second state comprising an SEU error signal.

8. A method according to claim 7 comprising producing an output of the second state from said comparison circuit in the absence of the original or the mirror result.

9. A method according to claim 7 further comprising inhibiting production of additional mirror results when said output is in the first state.

10. A method according to claim 9 further comprising performing an SEU recovery routine in response to detection of an SEU error signal.

11. A method according to claim 10 further comprising storing the original result and the mirror result in response to an SEU error signal, coupling the SEU error signal to command production of a next original result and a next mirror result, coupling said original result for comparison with said next original result by said comparison circuit and coupling said mirror result for comparison with said next mirror result by said comparison circuit and producing in said comparison circuit a signal of the first state when at least one of the original result and next original result or the mirror result and next mirror result match to allow use of a result matching a next result by said processor.

12. A method according to claim 11 wherein allowing use comprises transmitting the result to a processor bus.

13. A programmed medium which when executed on a processor performs the steps of: executing an original and mirror instructions to produce an original and a mirror result respectively to be compared in a redundancy routine, and receiving signals indicative of a comparison by a radiation hardened comparison circuit, and responding to an output of a first state from said comparison circuit when said original result agrees with said mirror result to treat the original result as true and responding to an output of a second state from said comparison circuit when said original result and said mirror result disagree, said second state comprising an SEU error signal, to treat the original result as not true.

14. A medium according to claim 13 further performing the step of inhibiting production of additional mirror results when said output is in the first state.

15. A medium according to claim 14 further performing the step performing an SEU recovery routine in response to detection of an SEU error signal.

16. A medium according to claim 15 further performing the steps of storing the original result and the mirror result in response to an SEU error signal, coupling the SEU error signal to command production of a next original result and a next mirror result, coupling said original result for comparison with said next original result by said comparison circuit and coupling said mirror result for comparison with said next mirror result by said comparison circuit and responding to producing in said comparison circuit a signal of the first state when at least one of the original result and next original result or the mirror result and next mirror result match to allow use of a result matching a next result by said processor.